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# ASIC Design Prototyping

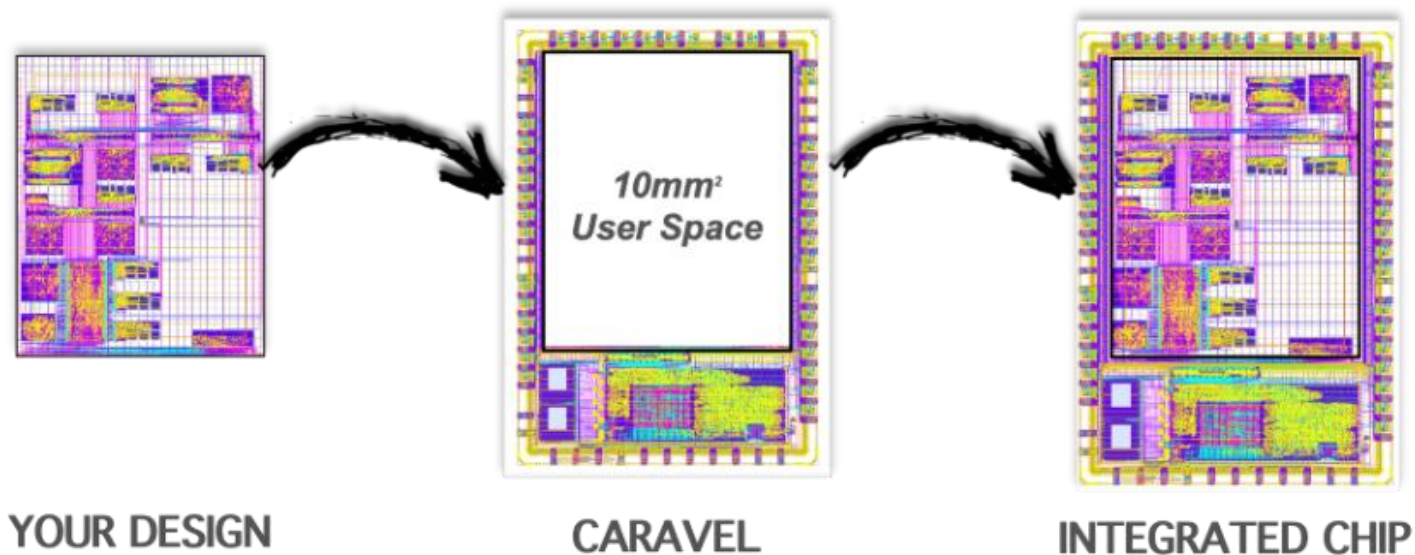
By: SDMAY25-28

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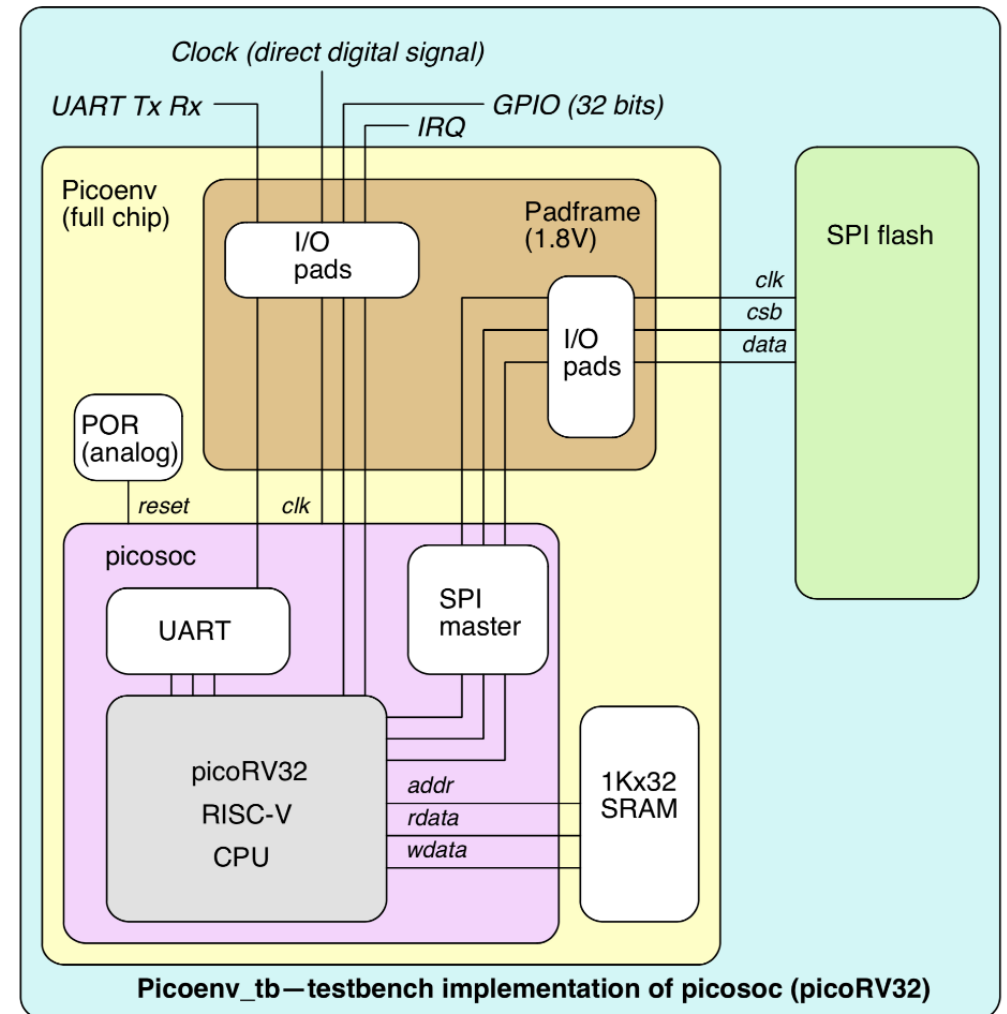
# Digital ASIC Design

- Digital ASIC (Application Specific Integrated Circuit)
- Implementing an RISC-V processor on chip
  - Extending the RISC-V ISA
  - Customizable ALU (Custom Logic Unit (CLU))
  - Designed in Verilog
- Fabricate on silicone using eFabless process



# ASIC Prototyping

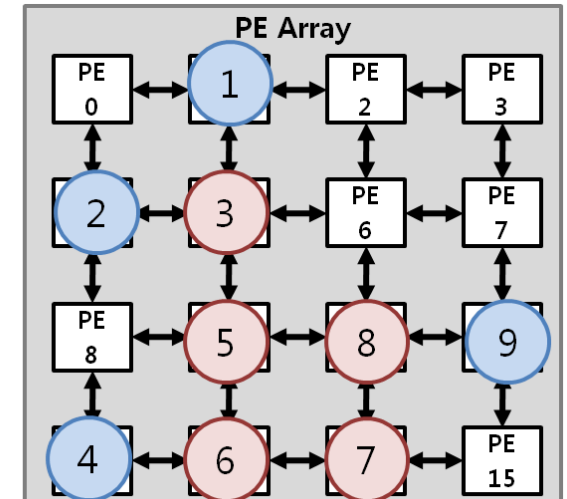
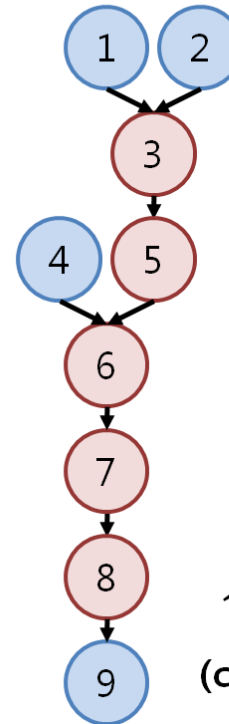
- How do we prototype?
  - Choosing our RISC-V processor
    - PICO RV
    - Rocket Chip
    - VexRiscV
  - Deciding on application
    - Application Accelerator
    - Eink Driver
  - High level design
    - How to communicate with the softcore
    - Ram?



# Reflection

- How did this improve our project?
  - Iterating on processors was good to learn about the different aspects of RISC-V soft cores
  - Gives us a better understanding of the RISC-V instruction set architecture
  - Learning about different applications let us understand what would work best for a general accelerator
    - Lead us to a Coarse-Grained Reconfigurable Architecture

(a) DFG from MPEG-2



(b) Mapping of DFG onto 4X4 CGRA

$$1^i, 2^i, 3^{i-1}, 4^{i-2}, 5^{i-2}, 6^{i-3}, 7^{i-4}, 8^{i-5}, 9^{i-6}$$

(c) Software Pipelined schedule with  $II = 1$

# Next Steps

- Iteration led us to slow down decision process
- Helped us choose better processor to fit our needs
- Next semester
  - Start iterating actual design on the accelerator
  - Continually improve the soft-core <-> caravel implementation

