Contextualization and Design Check-in

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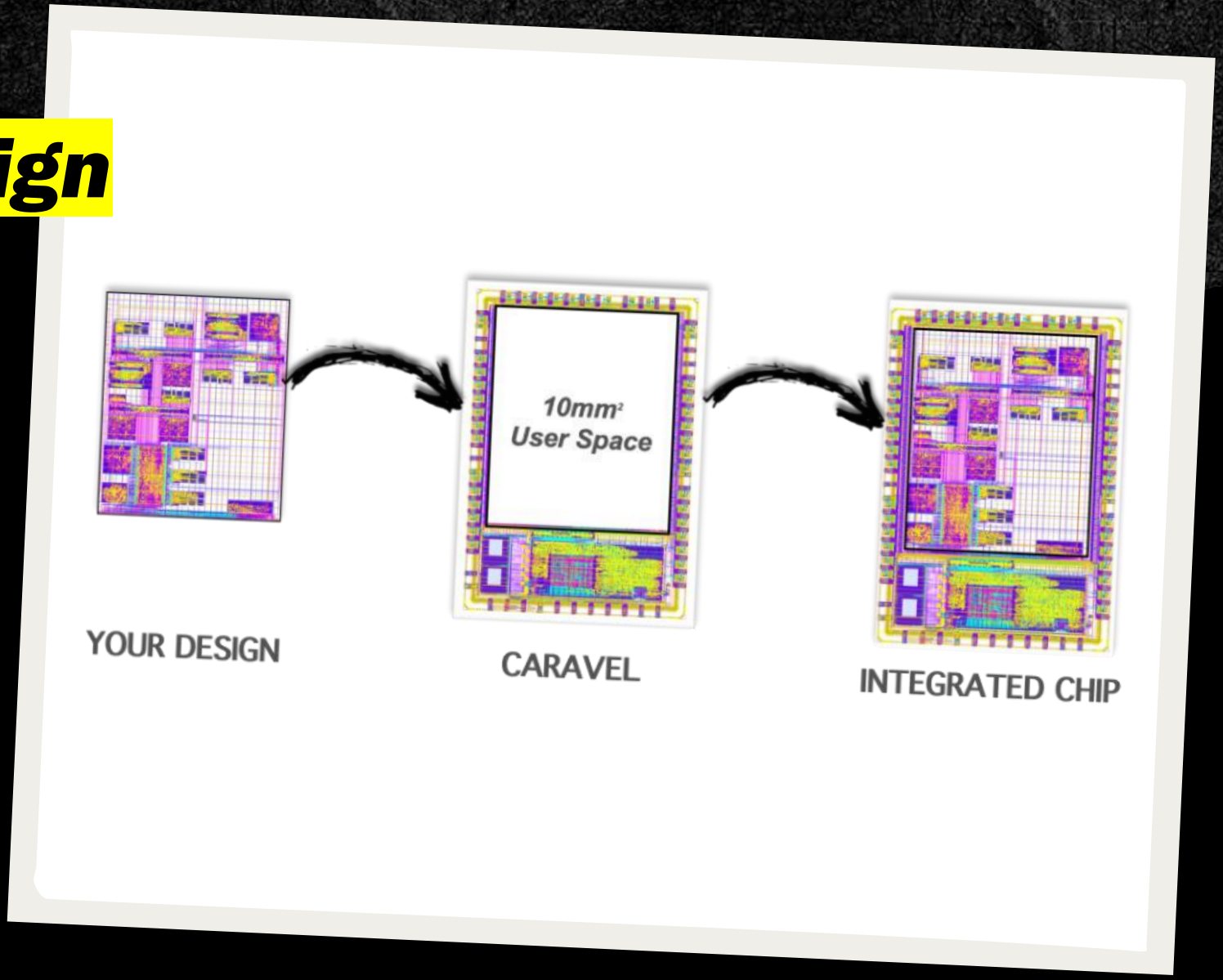
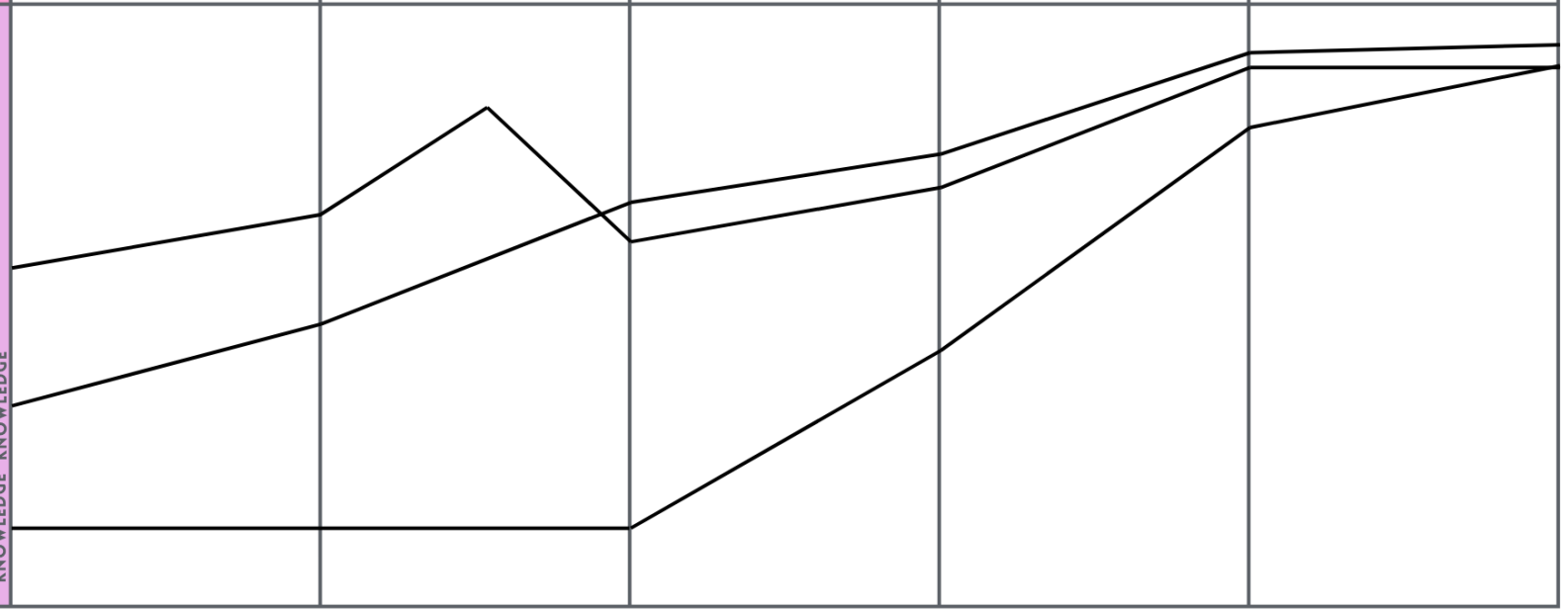
Digital ASIC Design

- Digital ASIC (Application Specific Integrated Circuit)
- Implementing an RISC-V processor on chip
  - Extending the RISC-V ISA
  - Customizable ALU (Custom Logic Unit (CLU))
  - Designed in Verilog
- Fabricate on silicone using eFabless process



Journey Map

HARDWARE STUDENT JOURNEY MAP

	DISCOVERY	LEARNING	DISCOVERY	LEARNING	PROFICIENCY
ACTIONS	Learns Computer Architecture	Starts to Learn Processor Design	Learns About Custom ISA Processor	Learns To Use Processor	Can Write Instruction and Programs for Processor
EXCITEMENT / PROCESSOR DESIGN KNOWLEDGE / CUSTOM ISA KNOWLEDGE					

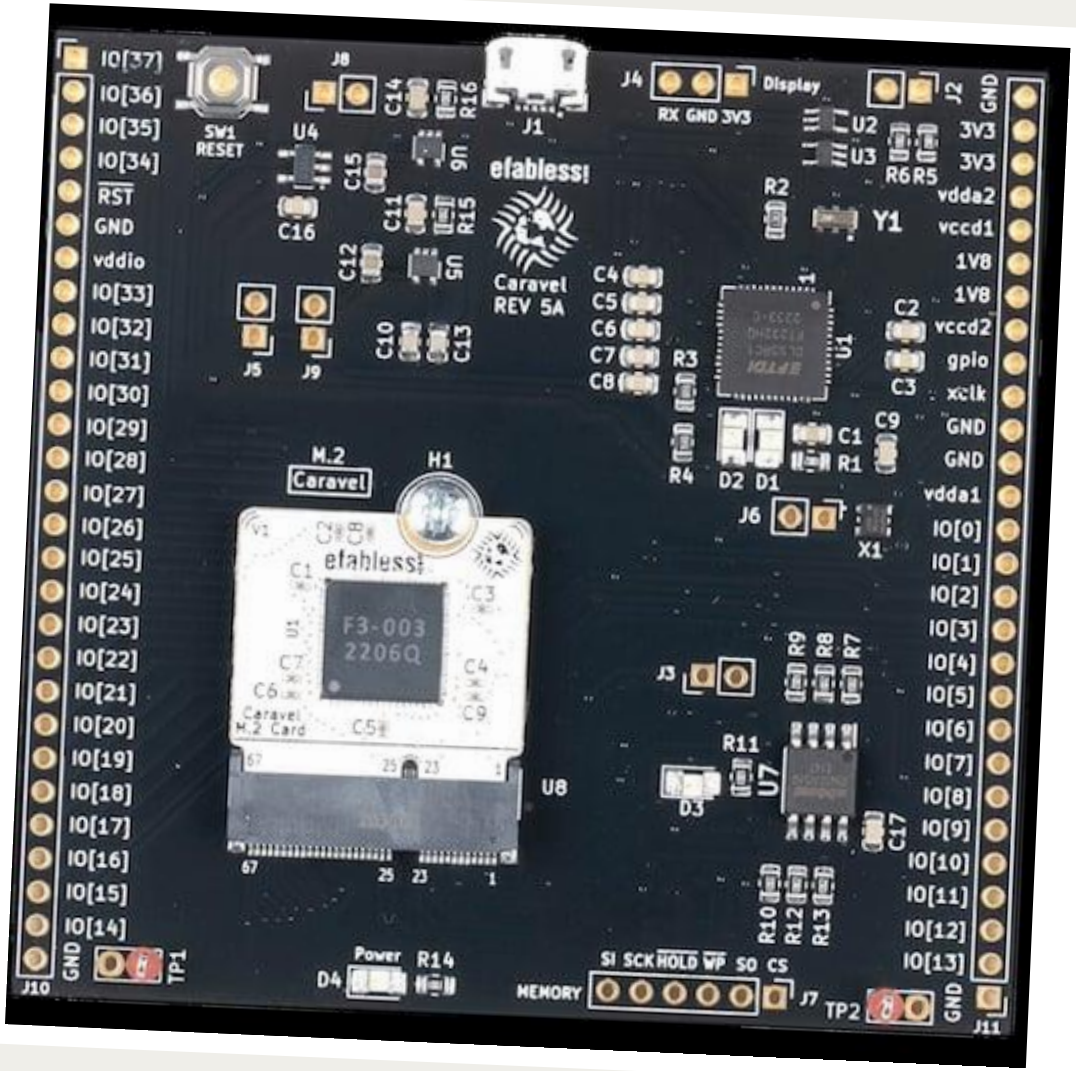
Pros/Cons Table

	Our solution	Arduino/ Rasberry Pi	Altera/Xilinx
Pros	– Free – Useful for learning computer architecture – Design documentation	– Cheap – Embedded Software – Widely used – Various ways to implement – Open-Source Projects	– Can be used to create many implementations – Useful for learning computer architecture – Open-Source Projects – Widely Used
Cons	– Limited documentation – Not widely used – Not many implementations	– Not free – Not helpful for learning computer architecture	– Expensive ($200+) – FPGA – Pretty big in size

Pros and Cons Table

Human

- Our current design implements many items to help address the user's needs
  - RISC-V SOC in user space for new members to program
  - Accelerator object that experienced members can utilize
  - Documentation to support users



Economic

- Improvements
  - Will be one of the first working chips back from efabless
  - Simple design for users to learn about
  - Ample documentation to read
- Drawbacks
  - Potential for chip to not work
    - Lots of checks before submitting to efabless and fabrication

Technical

- Internal Complexity
  - Simple RISC-V softcore
    - Choose a simple core to let students understand it better
    - Easier to modify or learn from for future projects
    - Similar design to caravel RISC-V core
- External Complexity
  - No additional complexity past the efabless caravel
  - Users will be able to apply knowledge of the external caravel and wrapper to all other ChipForge projects
  - Cannot modify the caravel