Detailed Design

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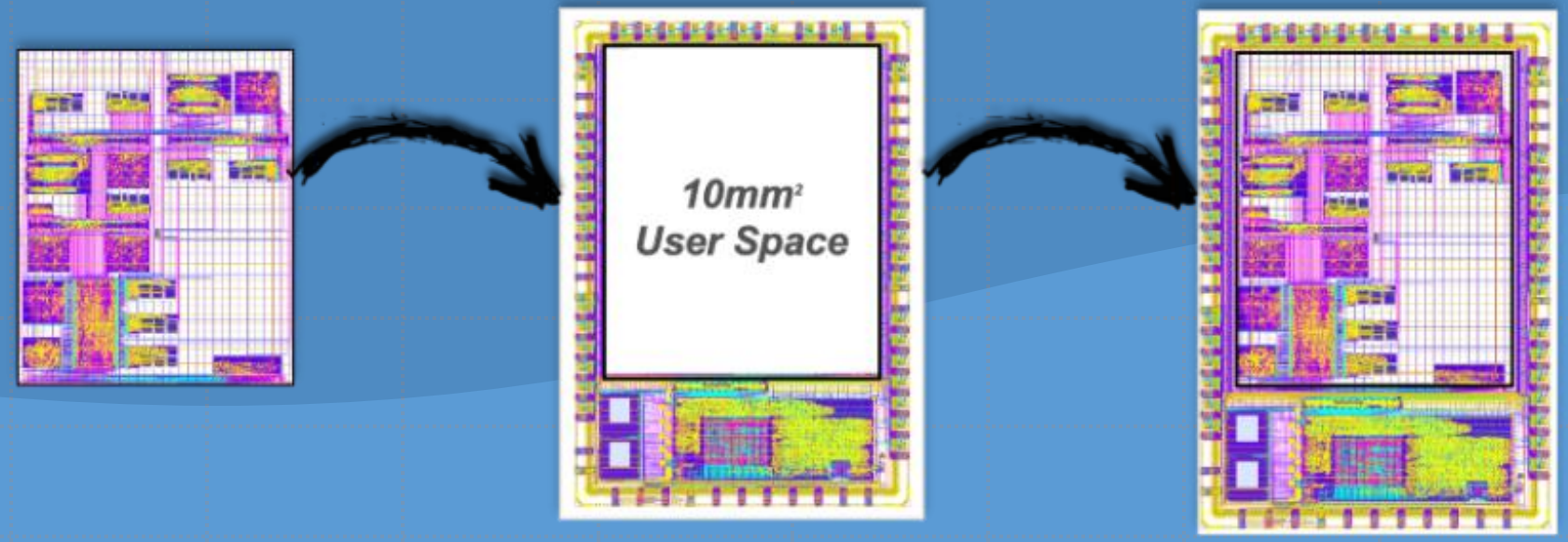
Client/Advisor: Dr Duwe

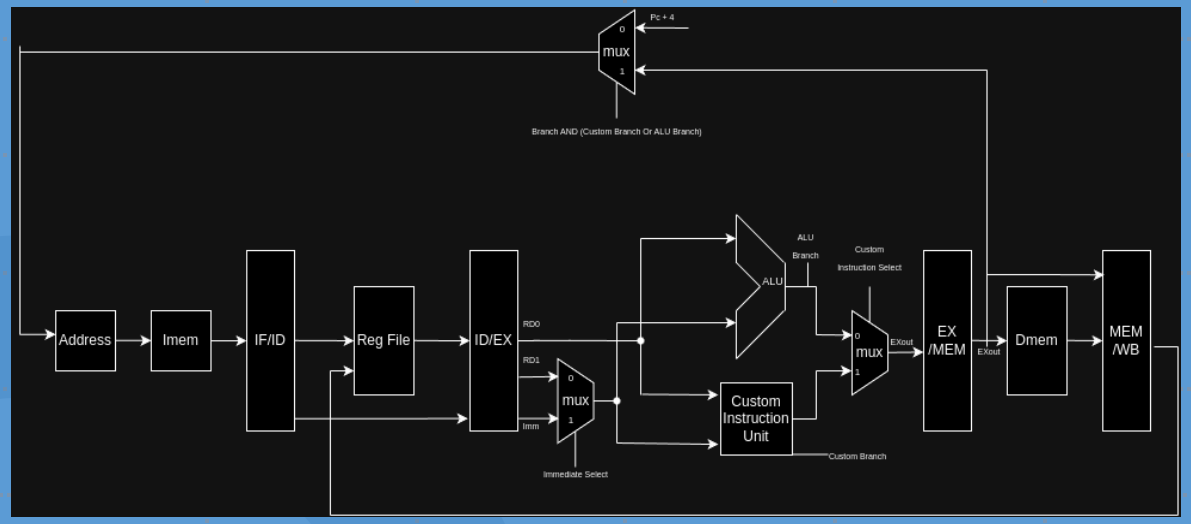


Digital ASIC Design

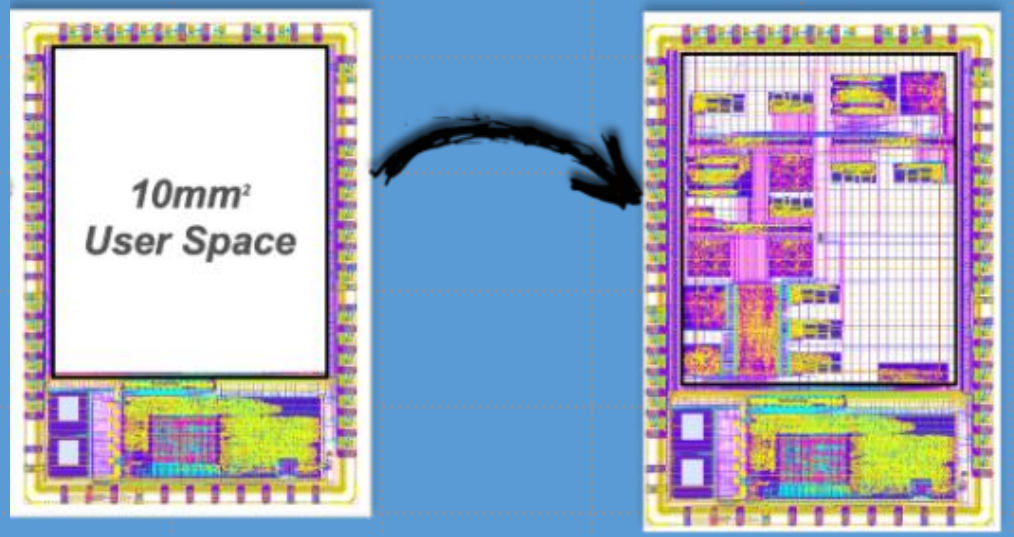
- Digital ASIC (Application Specific Integrated Circuit)
- Implementing an RISC-V processor on chip
  - Extending the RISC-V ISA
  - Customizable ALU (Custom Logic Unit (CLU))
  - Designed in Verilog
- Fabricate on silicone using eFabless process

Detailed Design

- Design and verify processor with Verilog
- Verify CLU (Custom Logic Unit) functions as designed



- Implement and harden design and verify for silicon fabrication within the caravel wrapper



Functionality

- RISC-V Processor
  - Basic RISC-V core using existing open source IP
  - Run and execute basic c programs
  - Modify ALU to implement CLU for custom instructions
- CLU (Custom Logic Unit)
  - Extend the RISC-V ISA (Instruction Set Architecture)
  - Allow programmability using CGRA (Coarse Grained Reconfigurable Architecture)
  - Work alongside RISC-V ALU to execute instructions

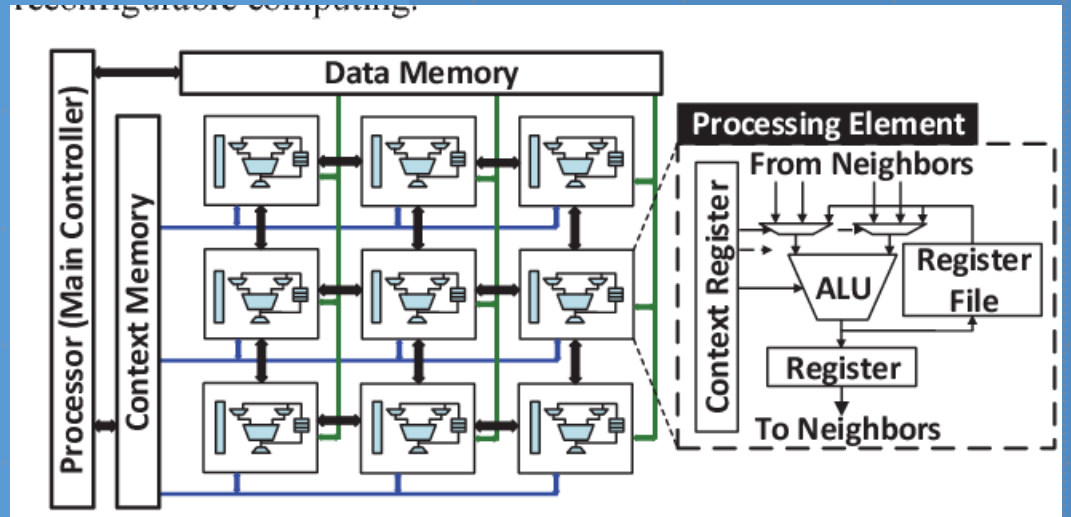


Fig. 1. Architectural Model of a typical 3x3 CGRA.

A. Motivating Example

Technology Considerations

- **CLU, CGRA or FPGA**
- CGRA (Coarse Grained Reconfigurable Architecture)
  - Configurable on the Word level
  - Fits our need for accelerating LLMs, which require lots of matrix multiplication and CGRAs excel at that
- FPGA (Field Reprogrammable Gate Array)
  - Configurable on the Bit level
  - Hyper specific configuration

- **Why RISC-V**
- RISC-V vs Others
  - Open source, which is one of our core requirements
  - Lots of existing projects and IP to build upon
  - Very customizable and flexible to fit our client needs

Areas of Concern/Development

- Fits the needs to support the ISU ChipForge Club
  - Reconfigurable and simple project that will allow younger students to learn on a simpler platform
  - Introduces what an ASIC is and how a custom chip is developed and behaves
  - Dr Duwe (Client) is happy with our current design and has approved it for further development

- Concerns relating to complexity of CGRA/CLU
  - Not quite sure how this will be implemented
  - Could take a whole team of 5 to complete in a semester potentially