User Needs and Requirements

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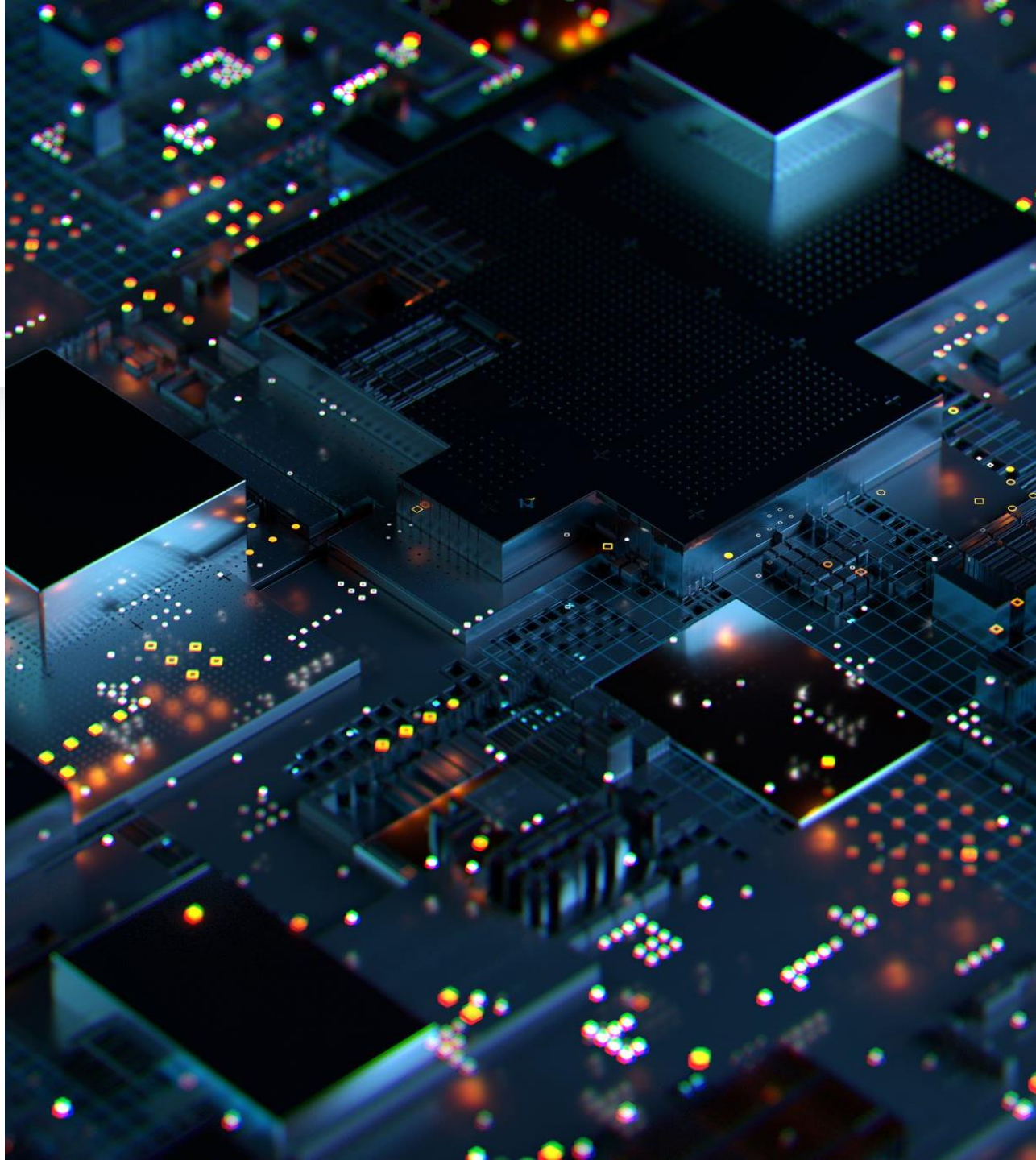
Project Overview

- Digital ASIC processor design
  - Create a custom RISC-V chip with a modifiable ALU with CGRA (course-grained reconfigurable architecture) to be able to add instructions to the RISC-V instruction set.
  - Output to eInk display connected through GPIO
  - Fabricate chip using efabless



User Needs

Chip Forge Club Members

- An interactive eFabless chip to get hands on experience with.
- Example eFabless chip(s) to jumpstart their own design.

Hardware Students

- A way to test new instructions for a RISC-V based instruction set.
- A way to test how these new instructions would work in a processor.
- A way to learn how ISAs work.

Professors

- A hands-on learning tool for RISC-V processors and their ISAs for students.
- A way to allow students to test their ideas on hardware.
- A way to allow processors to support instructions normal processors would not support.

Requirements

Functional

- Function as a RISC-V processor normally.
- Support custom instructions defined by the user.
- Custom instructions should only execute when called (should not execute when provided standard RISC-V instructions)

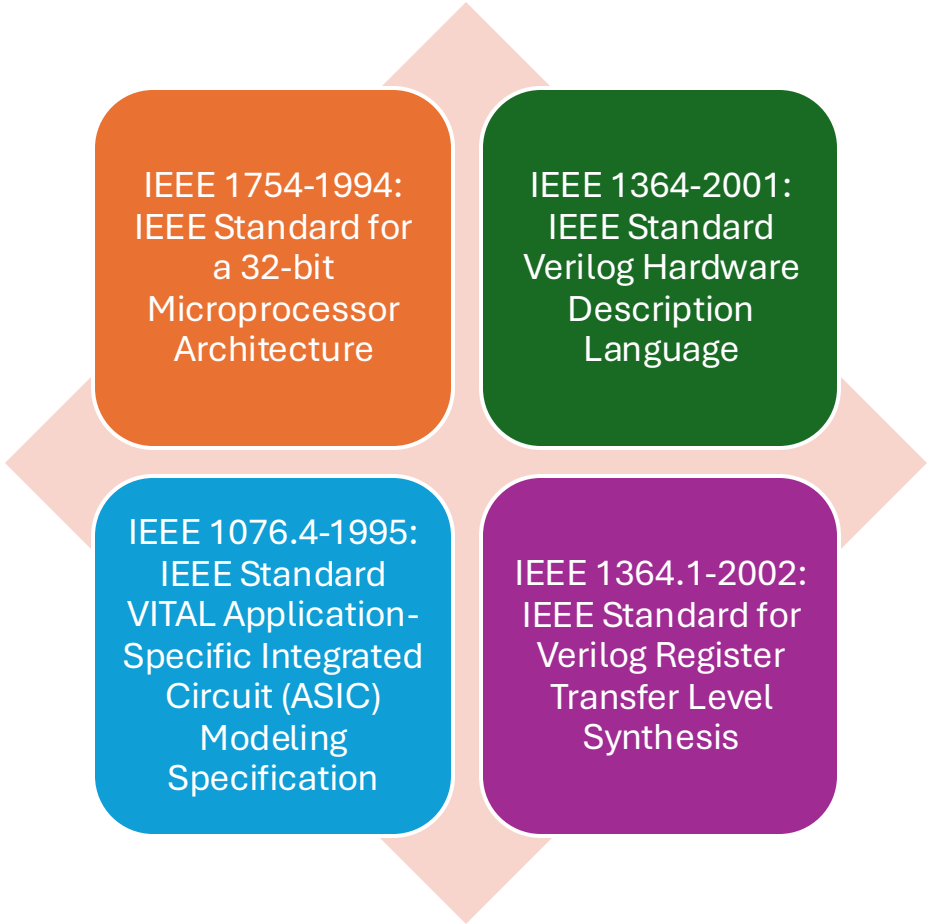
Technical

- HDL used is Verilog
- Custom instruction execution should not substantially slow down processer.
- Programming a new instruction should take minimal time.
- Be able to run at a clock frequency of 40 MHz.

User

- Should be user-friendly to program custom instructions and load in programs.
- Should have an advanced mode for more experienced users and a basic mode for inexperienced users.
- Should be easy to test custom instructions.

Engineering Standards



Conclusion

By adhearing to the requirements specificied. Our project should adequitly cover the needs of all our users. These requirements will also keep us on track and ensure we are doing what we need to do to be successful in this project.

We will also adhere to our listed IEEE standards to ensure our project remains consistent with the industry standard.